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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,549	01/21/2004	Masayoshi Tonouchi	ASAIN0137	8630

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,549	TONOUCHI ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3* is/are rejected.

7)☒ Claim(s) *2 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the examiner on form PTO-892 has cited the references, they have not been considered [see page 2, line 19-page 3, line 11, page 4, line 25-page 5, line 7].

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al (4906922) in view of Sakaguchi (5659244).

Regarding claim 1, Takahashi et al disclose [see Fig. 5] a method for inspecting wire breaking of a semiconductor integrated circuit (object under test 3) [see col. 4, lines 48-53] in a non-contact manner, comprising the steps of: maintaining a semiconductor integrated circuit in a state where a predetermined voltage is being applied thereto; two-dimensionally dimensional circuit (beam splitter 7) of scanning and irradiating a two-dimensional circuit of the semiconductor integrated circuit (3) by using an ultra short light pulse (via light source53) [light pulse not number but shown]; detecting [via detector 10] an electromagnetic wave [shown but not number] radiated from a position irradiated with the ultra short light pulse on the semiconductor integrated circuit (3); and detecting wire breaking of the irradiated position based on presence and absence or intensity of the electromagnetic wave [see col. 5, lines 41-66]. However, they do not disclose maintaining a semiconductor IC in a state where voltage is being applied as claimed. Sakaguchi discloses maintaining a semiconductor IC (target electronic circuit 100) in a state where voltage is being applied (via constant voltage supply 1) [see Abstract and col. 5, lines 22-51]. Further, Sakaguchi teaches that the addition of maintaining a semiconductor IC in a state where voltage is being applied is advantageous because it makes it possible to detect and identify failure sites and make measurement possible by utilizing the principle that a slight variation in electrical resistance of a wiring of a circuit varies magnitude of current supplied to that wiring. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Takahashi et al by adding constant voltage supply to the IC under test as taught by Sakaguchi in order to detect and identify failure sites and make measurement possible by utilizing the principle that a slight variation in electrical resistance of a wiring of a circuit varies magnitude of current supplied to that wiring.

Regarding claim 3, Takahashi et al disclose an apparatus [see Fig. 5] that inspects wire breaking of a semiconductor integrated circuit (object under test 3) [see col. 4, lines 48-53], comprising: a light pulse source (light source 53) that generates an ultra short light pulse [shown but not number]; a scanning device (beam splitter 7) that two-dimensionally scans and irradiates a two-dimensional circuit of the semiconductor integrated circuit (3) by using the ultra short light pulse; an electromagnetic wave detection device (detector 10) that detects an electromagnetic wave radiated from a position irradiated with the ultra short light pulse on the semiconductor integrated circuit (3); and wire breaking detection device (computer 11) that detects wire breaking of the irradiated position based on presence and absence or intensity of the electromagnetic wave. However, they do not disclose a voltage-applying device as claimed. Sakaguchi disclose [see Fig. 3] a voltage-applying device (constant voltage supply 1) that maintains a semiconductor integrated circuit (target electronic circuit 100) in a predetermined state where a voltage is being applied thereto [see Abstract and col. 5, lines 22-51]. Further, Sakaguchi teaches that the addition of maintaining a semiconductor IC in a state where voltage is being applied is advantageous because it makes it possible to detect and identify failure sites and make measurement possible by utilizing the principle that a slight variation in electrical resistance of a wiring of a circuit varies magnitude of current supplied to that wiring. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Takahashi et al by adding constant voltage supply to the IC under test as taught by Sakaguchi in order to detect and identify failure sites and make measurement possible by utilizing the principle that a slight variation in electrical resistance of a wiring of a circuit varies magnitude of current supplied to that wiring.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Koga (5701362), Taguchi et al (6661912) and Sunter (6717415) disclose a method and apparatus inspecting a device under test by using a light source.

6. Claims 2 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: regarding claims 2 and 4, the primary reason for the allowance of the claims is due to the specific limitation of the range for a wavelength, time average energy and a pulse width.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Patent Examiner
Art Unit 2829

JMH
April 13, 2005